Remarks/Arguments:

Claims 1-19 stand rejected.

Section 102/103 Rejections

Claims 1-19 have been rejected as anticipated by Boemler. Applicants respectfully submit that this rejection is overcome for the reasons set forth below.

Amended claim 1 now includes features which are not suggested by the cited reference, namely:

- wherein **the first and second banks of sample-and-hold circuits are directly connected to the pixel sensors**, and
- **the first and second analog-to-digital converters, respectively, are connected to the first and second banks of sample-and-hold circuits for independently digitizing the sampled succession of the reset and integrated voltages, respectively**.

Basis for amended claim 1 may be found, for example, in FIG. 6. As shown, there are two sample-and-hold circuits 610, 615 which are **directly connected to the pixel sensors**. In addition, the first and second analog-to-digital converters (ADCs) 650, 655 are, respectively, connected to the first and second sample-and-hold circuits 610, 615. Each ADC is configured to **independently** digitize the sampled succession of the reset and integrated voltages (sampled, respectively, by the first and second sample-and-hold circuits). Amended claim 1 now explicitly recites that **there are two sample-and-hold circuits and there are two ADCs for independently digitizing, respectively, the reset and integrated voltages provided from the two sample-and-hold circuits**.

Boemler, on the other hand, discloses a **single** digitizer connected to a pixel for converting an analog pixel value to a digital value. The digitizing is done twice by the same digitizer and the digital values are stored into two latches. As shown in FIG. 3, each digitizer provides a first digital output into latch 24 and then a second digital output into latch 124. One digitizer and two latches are used, per column.

Boemler does **not** suggest first and second banks of sample-and-hold circuits that are **directly connected to the pixel sensors**. Furthermore, Boemler does **not** suggest first and second ADCs that are, respectively, connected to the first and second banks of sample-and-hold circuits for **independently** digitizing the sampled succession of **the reset and integrated voltages, respectively** (as also recited, the first sample-and-hold circuit samples the reset voltages and second sample-and-hold circuit samples the integrated voltages).

Favorable reconsideration is respectfully requested for amended claim 1.

Dependent claims 2-7 depend from amended claim 1 and are, therefore, not subject to rejection in view of the cited reference for at least the same reasons set forth for amended claim 1.

Claim 8

Although not the same, Claim 8 has been amended to include features similar to amended claim 1, namely:

(b) **sampling and holding reset voltages** of the selected pixel sensors; ...

(d) **sampling and holding integrated voltages** of the selected pixel sensors...;

sampling and holding the reset voltages is performed by the first channel only and **sampling and holding the integrated voltages is performed by the second channel only**, and

converting the reset and integrated voltages into digital reset and integrated values is **performed after the sampling and holding** of the reset and integrated voltages, respectively.

As shown in FIG. 6, for example, sample-and-hold circuits 610, 615 provide analog outputs of the reset and integrated voltage values, respectively. The ADCs 650, 655 digitize the reset and integrated voltage values, after the sample and hold circuits have performed their respective tasks.

Boemler, as described above, twice digitizes the pixel voltage outputs by the same digitizer (first, digitizing the reset voltages and, second, digitizing the integrated voltages);

next, Boemler provides two latches for storage of the digitized values. Boemler, however, does **not** suggest providing first and second sample and hold circuits for initially sampling the reset and integrated values and then, next, providing first and second ADCs for converting the reset and integrated voltages into digital reset and integrated values, respectively.

Favorable reconsideration is requested for amended claim 8.

Dependent claims 9-18 depend from amended claim 8 and are, therefore, not subject to rejection in view of the cited reference for at least the same reasons set forth for amended claim 8.

Conclusion

The application is now in condition for allowance.

Respectfully submitted,

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